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10/697,503	10/30/2003	David A. Luick	ROC920020009US1	8053

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EXAMINER	
YU, JAE UN	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/697,503	LUICK, DAVID A.	
	Examiner	Art Unit	
	Jae U. Yu	2185	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *25 April 2007*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *2-8,10-14,17 and 19* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *2-8, 10-14, 17 and 19* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

The examiner acknowledges the applicant's submission of the amendment dated 4/25/2007. At this point claim 17 has been amended and claims 1, 9, 15, 16 and 18 have been cancelled. Claim 19 has been added. Thus, claims 2-8, 10-14, 17 and 19 are pending in the instant application.

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 2-5, 10-13, 17 and 19 are rejected under 35 U.S.C. 103 (a) as being obvious over Peir et al. (US 2003/0208665 A1) in view of Au (US 5,548,795).

2. As per **independent claims 17 and 19**, Pier et al. disclose, "at least one pipeline **[Figure 1]** able to selectively load, execute **["Load, Execute", Paragraph 11]** and flush as series of instructions **[Selectively canceling dependent instructions, Figure 3]**".

"at least one fast-load data cache that loads at least one speculative data load relative to the speculative instruction into the pipeline" **Peir et al. discloses the cache (110) in Figure 1, and the "cache hit" determination step in Figure 3**. If there is a cache hit,

data must, inherently, have been loaded into the cache relative to the speculative instruction.

"at least one L1 data cache **["L2 Cache", Figure 1]** that holds at least one non-speculative data load, corresponding to the speculative instruction, into the pipeline a predetermined number of cycles **[L2 lookup, Paragraph 16]** after the fast-load data cache loads the speculative data load **[loading results in the "hit" determination step, Figure 3]**"

"A circuit that determines if the speculative data load is a misprediction **[The computer system determines cache hit/miss, Figure 3]**"

"if the speculative load is a misprediction **[Cache Miss, Figure 3]**, the pipeline to inhibit execution of the speculative load and any instructions dependent thereon **[Canceling dependent instruction 330, Figure 3]** and to execute the non-speculative load and any instructions dependent thereon **[miss request to the L2 cache, paragraph 16]**; and if the speculative load is not a misprediction, the pipeline to execute the speculative load an any instructions dependent thereon **[Continue executing the dependent instruction, Figure 3]** and to inhibit the non-speculative load and any instructions dependent thereon **[inhibit the miss request to the L2 cache, Paragraph 16]**"

Peir et al. discloses keeping track of speculative load dependency, as disclosed above. However, Peir et al. does not disclose expressly the limitation, "selectively flagging each of the series of instructions with a flag to indicate dependence".

Au discloses, **"The D_Flag fields 308 in each record 202 indicate dependency relative to a more forward command record 202" in column 8, at lines 44-46 and in Figure 3.**

Peir et al. and Au are analogous art because they are from the same field of endeavor of determining and processing data/instructions that are dependent on other data/instructions.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. by including the step of setting a flag bit as taught by Au in column 8, at lines 44-46.

The motivation for doing so would have been to "maintain all command dependencies in a graph structure to reduce the number of address overlap-checks required" as expressly taught by Au in column 7, at lines 14-15.

Therefore, it would have been obvious to combine Au with Peir et al. for the benefit of command dependency indication to obtain the invention as specified in claims 17 and 19.

3. As per **claims 2 and 10**, "the speculative data load is loaded in the pipeline." **Peir et al. discloses, "The processor 100 may establish a cache hit/miss prediction table (CPT) to record the hit/miss history of memory references and use the CPT to predict cache hit/miss for future memory reference" in paragraph 13.** The "processor" corresponds to the "pipelines" from the claim, and the "CPT" corresponds to the "speculative data" from the claim.

4. As per **claims 3 and 11**, "one or more of the data loads in the pipeline are not dependent on any specific data load and not selectively flagged." **Peir et al. discloses, "Independent instructions scheduled during this one cycle window may be allowed to continue regardless" in paragraph 16.** Independent instructions ("the data loads that are not dependent" from the claim) are always executed and flagging them is inherently unnecessary.

5. As per **claims 4 and 12**, Peir et al. and Au disclose the system recited in claim 1.

Au discloses, in **Figure 3**, the "D_Flag" field 308 within "Command Record" 202. Record 202 corresponds to the "instruction" from the claim. The "D_Flag" is a bit since it represents a bistate field **(Column 7, Lines 46-48).**

6. As per **claims 5 and 13**, Peir et al. and Au disclose the system recited in claim 1.

Au discloses, in **Figure 3,** the "D_Flag" field 308 attached to the "Logical Block Address" 302 and 304. The "Logical Block Addresses" correspond to the "data load"

from the claim. In addition, examiner notes that mere separation of parts (i.e. flags and data load) is not a patentable distinction over the prior art. See MPEP 2144.04 (C).

7. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peir et al. and Au as applied to claim 1 above, and further in view of "The Cache Memory Book" by Jim Handy.

8. As per **claim 7**, Peir et al. and Au disclose the system recited in claim 1. However, Peir et al. and Au do not disclose expressly the limitation "the fast-load data cache includes a directory".

In paragraph 27 of the Applicant's specification, it is disclosed that a directory can be omitted if the cache is a one-way associate or direct-map cache. **Handy discloses a two-way associative cache in Page 54, at lines 23-25.** Since the cache is not a one-way associate or direct-map cache, it inherently includes a directory.

Peir et al., Au and Handy are analogous art because they are from the same field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. and Au by including the two-way associative cache as taught by Handy in Page 54.

The motivation for doing so would have been the high hit rate of the small size two-way associative cache as expressly taught by Handy in Page 55, Figure 2.9.

Therefore, it would have been obvious to combine Peir et al. and Au with Handy for the benefit of high cache hit rate to obtain the invention as specified in claim 7.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Peir et al. and Au as applied to claim 1 above, and further in view of "The Cache Memory Book" by Jim Handy.

10. As per **claim 8**, Peir et al. and Au disclose the system recited in claim 1. However, Peir et al. and Au do not expressly disclose the limitation "the fast-load data cache does not include a directory."

Sato et al. discloses **"A set of routines which are frequently used in an OS is stored in a local memory arranged in a CPU and having high-speed elements" in column 2, at lines 23-26,** wherein the "local memory" corresponds to the "fast-load data cache" from the claim. Sato et al. also discloses **"A local memory which has part of address locations of the main memory as its address location, which is accessed by a CPU, and which can obtain same effect as cache memory without having cache directory" in the Abstract.**

Peir et al., Au and Sato et al. are analogous art because they are from the same field of endeavor of computer storage access/management.

At the time of the invention it would have been obvious to a person of ordinary skill in the art to modify Peir et al. and Au by including the high-speed "local memory" without cache directory as taught by Sato et al. in column 2, at lines 23-26 and in the Abstract.

The motivation for doing so would have been the improved bus performance as expressly taught by Sato et al. in column 2, at lines 27-30.

Therefore, it would have been obvious to combine Peir et al. and Au with Handy for the benefit of improved bus performance to obtain the invention as specified in claim 8.

11. Claims 6 and 14 are rejected under 35 U.S.C. 103(a) as being unpatentable over Peir et al. (US 2003/0208665 A1) and Au (US 5,548,795) as applied to claims 17 and 18 above, and further in view of Kyker et al. (US 6,467,027).

12. As per **claims 6 and 14**, Peir et al. and Au disclose canceling "each flagged instruction from the pipeline upon the determination of a misprediction for a data load" in Figure 3 (Peir et al.).

Peir et al. and Au do not disclose expressly that "canceling instructions" corresponds to "flushing instructions".

Kyker et al. disclose instruction flush in column 9, at lines 16-21.

Peir et al., Au and Kyker et al. are analogous art because they are from the same filed of endeavor of instruction processing.

At the time of the invention it would have been to a person of ordinary skill in the art to modify Peir et al. and Au by including instruction flush as taught by Kyker et al. in column 9, at lines 16-21.

The motivation for doing so would have been to allow "process switch" as expressly taught by Kyker et al. in column 9, at lines 16-21.

Therefore, it would have been obvious to combine Kyker et al. with Peir et al. and Au for the benefit of allowing process switch to obtain the invention as specified in claims 6 and 14.

Arguments Concerning Prior Art Rejections

1st Point of Argument

Regarding independent claims 17 and 19, the applicant argues that the combination of Pier et al. and Au do not teach the amended limitation, "if the speculative load is a misprediction, execute the non-speculative load and any instructions dependent thereon". However, Pier et al. teaches if the speculative load is incorrectly predicted, only the instructions dependent on the speculative load are cancelled in Figure 3 and Paragraph 18. Thus, any loads/instructions not dependent on the speculative load are not flushed and executed thereon.

Conclusion

THIS ACTION IS MADE FINAL. Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

A. Claims Rejected in the Application

Claims 2-8, 10-14, 17 and 19 have received a fourth action on the merits and are subject of a fourth action final.

B. Direction of Future Remarks

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jae Un Yu who is normally available from 9:00 A.M. to 5:30 P.M. Monday thru Friday and can be reached at the following telephone number: (571) 272-1133.

If attempts to reach the above noted examiner by telephone are unsuccessful, the Examiner's supervisor, Sanjiv Shah, can be reached at the following telephone number: (571) 272-4098.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

July 7, 2007

Jae Un Yu

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